WHAT IS CLAIMED IS:

1. An electrostatic discharge protection circuit, comprising:

a rectifier, having an anode and a cathode, including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, and a second n-type portion contiguous with the second p-type portion, wherein the first p-type portion is coupled to the anode and the second n-type portion is coupled to the cathode;

a first transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the first n-type portion of the rectifier;

a second transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the second terminal of the first transistor, and the second terminal is coupled to the second n-type portion of the rectifier; and

a voltage coupling circuit having a first terminal, a second terminal, a third terminal, and a fourth terminal, wherein the first terminal is coupled to the anode of the rectifier, the second and the third terminals are respectively coupled to the gate terminals of the first and second transistors, and the fourth terminal is coupled to the cathode.

2. The circuit as claimed in claim 1, wherein the voltage coupling circuit provides a first voltage signal to the gate of the first transistor and a second voltage signal to the gate of the second transistor to turn on the rectifier.

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FINNEGAN, HENDERSON,
FARABOW, GARRETT,
& DUNNER, L.L.P.
901 NEW YORK AVENUE, N. W.
WASHINGTON, DC 20005
202-408-4000

3. The circuit as claimed in claim 2, wherein the voltage coupling circuit includes a first capacitor coupled to the first terminal of the voltage coupling circuit and the gate terminal of the first transistor, and a second capacitor coupled to the first terminal of the voltage coupling circuit and the gate terminal of the second transistor.

4. The circuit as claimed in claim 3, wherein the voltage coupling circuit further includes a third transistor having a source, a drain and a gate, the drain of the third transistor coupled to the gate of the first transistor and the source of the third transistor coupled to the gate of the first transistor.

5. The circuit as claimed in claim 3, wherein the voltage coupling circuit further includes a clamping circuit, a first resistor and a second resistor, the clamping circuit coupled to the first resistor and the gate terminal of the first transistor, and the first resistor coupled to the clamping circuit and the cathode of the rectifier, and the second resistor coupled to the gate terminal of the second transistor and the cathode of the rectifier.

6. The circuit as claimed in claim 5, wherein the clamping circuit clamps the first voltage signal provided to the gate terminal of the first transistor, and the first and second resistors, in conjunction with the first and second capacitors, control a time delay to turn on the rectifier.

7. The circuit as claimed in claim 5, wherein the clamping circuit comprises a transistor.

8. The circuit as claimed in claim 1, wherein the second p-type portion of the rectifier comprises a p-type semiconductor substrate.

9. The circuit as claimed in claim 1, wherein the first n-type portion of the rectifier comprises an n-well in a semiconductor substrate.

10. The circuit as claimed in claim 8, wherein the first n-type portion of the rectifier includes an n-well in the semiconductor substrate, and the first p-type portion of the rectifier includes a p-type diffused region inside the n-well.

11. The circuit as claimed in claim 10, wherein the second n-type portion of the rectifier comprises an n-type diffused region inside the semiconductor substrate and spaced apart from the first n-type portion.

12. The circuit as claimed in claim 5, wherein the voltage coupling circuit further includes a fourth transistor having a source, a drain and a gate, the drain coupled to the gate of the second transistor, the gate coupled to the drain of the third transistor, and the source coupled to the cathode.

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)UNNER, L.L.P.
I STREET, N.W.
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13. An integrated circuit, comprising:

a signal pad for receiving and outputting a signal;

a rectifier with an anode and a cathode including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, and a second n-type portion contiguous with the second p-type portion, wherein the anode of the rectifier is coupled to the signal pad;

a first transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the first n-type portion of the rectifier; and

a second transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the second n-type portion of the rectifier, and the second terminal is coupled to the second terminal of the first transistor.

14. The circuit as claimed in claim 13 further comprising a voltage coupling circuit coupled to the gate terminals of the first and second transistors.

15. The circuit as claimed in claim 13, wherein the anode is coupled to the first p-type portion.

16. The circuit as claimed in claim 13, wherein the anode is coupled to the second n-type portion.

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& DUNNER, L.L.P.
901 NEW YORK AVENUE, N. W.
WASHINGTON, DC 20005
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17. The circuit as claimed in claim 14, wherein the voltage coupling circuit provides a first voltage signal to the gate of the first transistor and a second voltage signal to the gate of the second transistor to turn on the rectifier.

18. The circuit as claimed in claim 14, wherein the voltage coupling circuit includes a first capacitor coupled to the gate terminal of the first transistor and a second capacitor coupled to the gate terminal of the second transistor.

19. The circuit as claimed in claim 18, wherein the first capacitor and the second capacitor are coupled to the signal pad.

20. The circuit as claimed in claim 18, further comprising an output buffer having a first terminal and a second terminal, wherein the first terminal is coupled to the signal pad and the second terminal is coupled to the first capacitor and the second capacitor.

21. The circuit as claimed in claim 20, wherein the output buffer comprises a transistor, wherein the second terminal is coupled to an n-well of the transistor.

22. The circuit as claimed in claim 16, wherein the voltage coupling circuit further comprises a clamping circuit to clamp the first voltage signal provided to the gate terminal of the first transistor.

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DUNNER, L.L.P.
I STREET, N. W.
NGTON, DC 20005
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23. The circuit as claimed in claim 13, wherein the second p-type portion of the rectifier comprises a p-type semiconductor substrate.

24. The circuit as claimed in claim 13, wherein the first n-type portion of the rectifier comprises an n-well in a semiconductor substrate.

25. The circuit as claimed in claim 23, wherein the first n-type portion of the rectifier comprises an n-well in the semiconductor substrate, and the first p-type portion comprises a p-type diffused region inside the n-well.

26. An integrated circuit, comprising:

a signal pad for receiving and outputting a signal;

an output buffer having a first terminal and a second terminal, wherein the second terminal is coupled to the signal pad;

a rectifier, having an anode and a cathode, including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, and a second n-type portion contiguous with the second p-type portion, wherein the first p-type portion is coupled to the anode, the second n-type portion is coupled to the cathode, the anode is coupled to the first terminal of the output buffer, and the cathode is coupled to ground;

a first transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the first n-type portion of the rectifier;

a second transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the second terminal of the first transistor, and the second terminal is coupled to the second n-type portion of the rectifier; and

a voltage coupling circuit having a first terminal, a second terminal, a third terminal and a fourth terminal, wherein the first terminal is coupled to the anode of the rectifier, the second and the third terminals are respectively coupled to the gate terminals of the first and second transistor, and the fourth terminal is coupled to the cathode of the rectifier.

27. The circuit as claimed in claim 26, wherein the voltage coupling circuit provides a first voltage signal to the gate of the first transistor and a second voltage signal to the gate of the second transistor to turn on the rectifier.

28. The circuit as claimed in claim 27, wherein the voltage coupling circuit includes a first capacitor coupled to the first terminal of the voltage coupling circuit and the gate terminal of the first transistor, and a second capacitor coupled to the first terminal of the voltage coupling circuit and the gate terminal of the second transistor.

29. The circuit as claimed in claim 28, wherein the voltage coupling circuit further includes a third transistor having a source, a drain and a gate, the drain being coupled to the gate and the source being coupled to the gate of the first transistor.

30. The circuit as claimed in claim 28, wherein the voltage coupling circuit further includes a clamping circuit, a first resistor and a second resistor, the clamping circuit coupled to the first resistor and the gate terminal of the first transistor, and the first resistor coupled to the clamping circuit and the cathode of the rectifier, and the second resistor coupled to the gate terminal of the second transistor and the cathode of the rectifier.

31. The circuit as claimed in claim 30, wherein the clamping circuit clamps the first voltage signal provided to the gate terminal of the first transistor, and the first and second resistors and the first and second capacitors control a time delay to turn on the rectifier.

32. The circuit as claimed in claim 30, wherein the clamping circuit comprises a transistor.

33. The circuit as claimed in claim 26, wherein the second p-type portion of the rectifier comprises a p-type semiconductor substrate.

34. The circuit as claimed in claim 26, wherein the first n-type portion of the rectifier comprises an n-well in a semiconductor substrate.

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) I STREET, N. W.
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35. The circuit as claimed in claim 33, wherein the first n-type portion of the rectifier comprises an n-well in the semiconductor substrate, and the first p-type portion of the rectifier comprises a p-type diffused region inside the n-well.

36. The circuit as claimed in claim 35, wherein the second n-type portion of the rectifier comprises an n-type diffused region inside the semiconductor substrate and spaced apart from the first n-type portion.

37. The circuit as claimed in claim 30, wherein the voltage coupling circuit further includes a fourth transistor having a source, a drain and a gate, the drain coupled to the gate of the second transistor, the gate coupled to the drain of the third transistor, and the source coupled to the cathode.

38. An integrated circuit, comprising:

a signal pad for receiving and outputting a signal;

an output buffer having a first terminal and a second terminal, wherein the second terminal is coupled to the signal pad;

a rectifier with an anode and a cathode including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, and a second n-type portion contiguous with the second p-type portion, wherein the anode of the rectifier is coupled to the second terminal of the output buffer and the cathode of the rectifier is coupled to ground;

a first transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the first n-type portion of the rectifier;

a second transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the second terminal of the first transistor, and the second terminal is coupled to the second n-type portion of the rectifier; and

a voltage coupling circuit having a first terminal, a second terminal, a third terminal and a fourth terminal, wherein the first terminal is coupled to the first terminal of the output buffer, the second and the third terminals are respectively coupled to the gate terminals of the first and second transistor, and the fourth terminal is coupled to the cathode of the rectifier.

39. The circuit as claimed in claim 38, wherein the voltage coupling circuit provides a first voltage signal to the gate of the first transistor and a second voltage signal to the gate of the second transistor to turn on the rectifier.

40. The circuit as claimed in claim 39, wherein the voltage coupling circuit includes a first capacitor coupled to the first terminal of the voltage coupling circuit and the gate terminal of the first transistor, and a second capacitor coupled to the first terminal of the voltage coupling circuit and the gate terminal of the second transistor.

41. The circuit as claimed in claim 40, wherein the voltage coupling circuit further includes a third transistor having a source, a drain and a gate, the drain coupled to the gate and the source coupled to the gate of the first transistor.

42. The circuit as claimed in claim 40, wherein the voltage coupling circuit further includes a clamping circuit, a first resistor and a second resistor, the clamping circuit coupled to the first resistor and the gate terminal of the first transistor, and the first resistor couple to the clamping circuit and the cathode of the rectifier, and the second resistor coupled to the gate terminal of the second transistor and the cathode of the rectifier.

43. The circuit as claimed in claim 42, wherein the clamping circuit clamps the first voltage signal provided to the gate terminal of the first transistor, and the first and second resistors and the first and second capacitors control a time delay to turn on the rectifier.

44. The circuit as claimed in claim 42, wherein the clamping circuit comprises a transistor.

45. The circuit as claimed in claim 38, wherein the second p-type portion of the rectifier comprises a p-type semiconductor substrate.

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DUNNER, L.L.P.
I STREET, N. W.
NGTON, DC 20005
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46. The circuit as claimed in claim 38, wherein the first n-type portion of the rectifier comprises an n-well in a semiconductor substrate.

47. The circuit as claimed in claim 45, wherein the first n-type portion of the rectifier comprises an n-well in the semiconductor substrate, and the first p-type portion of the rectifier comprises a p-type diffused region inside the n-well.

48. The circuit as claimed in claim 47, wherein the second n-type portion of the rectifier comprises an n-type diffused region inside the semiconductor substrate and spaced apart from the first n-type portion.

49. The circuit as claimed in claim 42, wherein the voltage coupling circuit further includes a fourth transistor having a source, a drain and a gate, the drain coupled to the gate of the second transistor, the gate coupled to the drain of the third transistor, and the source coupled to the cathode.

50. A method for protecting an integrated circuit with a dual input/output pad from electrostatic discharge, comprising:

providing a rectifier having a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first n-type portion, and a second n-type portion contiguous with the second p-type portion;

providing a first transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the first n-type portion of the rectifier; and

providing a second transistor having a first terminal, a second terminal and a gate terminal, wherein the first terminal is coupled to the second terminal of the first transistor, and the second terminal is coupled to the second n-type portion of the rectifier.

51. The method as claimed in claim 50, further comprising a step of providing a first voltage signal to the gate of the first transistor and a second voltage signal to the gate of the second transistor to turn on the rectifier.